In the Specification

Delete the paragraph beginning on page 3, line 15, and replace it with the following paragraph:

Preferably, the semiconductor substrate is a silicon substrate having a pad dielectric layer thereover a surface of the silicon substrate. More preferably, the semiconductor substrate is a silicon substrate having a pad dielectric layer comprising a pad oxide layer followed by a pad nitride layer thereover the surface of the silicon substrate. The pad oxide layer may be provided to a thickness ranging from about 1 to about 10 nm, while the pad nitride may be provided to a thickness ranging from about 50 to about 500 nm. In such an embodiment, the plurality of trenches formed in the substrate traverse through the pad oxide and pad nitride layers, stopping at a distance within the silicon substrate. Preferably the plurality of trenches are etched to a depth ranging from about 250 nm to about 10μm.

Delete the paragraph beginning on page 20, line 20, and replace it with the following paragraph:

Next, as illustrated in Fig. 12, a trench gate electrode material 280 such as LPCVD silicon may be deposited over the substrate to at least fill the empty portions of the trenches 18. The trench gate electrode material 280 is then planarized to a top surface of the pad nitride layer 15, thereby removing any trench-top oxide 250 remaining over

the surface of the pad nitride layer 15, as illustrated in Fig. 13B. ~~A s~~Shallow trench isolations (STI) 285 may then be formed in the substrate. As illustrated in the top plane view of Fig. 13A and in the partial cross sectional view of Fig. 13B along the dashed line 202 in Fig. 13A, the STIs 285 are formed therebetween the adjacent active rows 45 of paths of trenches 42. The STIs 285 are formed by known techniques including photolithography, dry etch, HDP oxide deposition, planarization, and the like to a depth ranging from about 300nm to about 600nm, preferably to about 400nm. In the present invention, the STIs 285, as shown in Fig. 13B, are formed to provide isolation for the IC transistors in the peripheral regions of the transistor and to isolate the adjacent memory cells in the arrays. The STI 285 will be substantially perpendicular in orientation in relation to the merged isolation regions 30 as shown in Fig. 6, thereby providing isolation for individual memory cells.